Integrated Silicon PIN Photodiodes Using Deep N-Well in a Standard 0.18-μm CMOS Technology

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Abstract—This paper studies integrated silicon photodiodes (PDs) implemented in standard CMOS technologies. A new PIN PD structure utilizing deep n-well is presented, and compared with conventional vertical and lateral PIN PDs at 850-nm wavelength and different bias conditions. Prototype PDs were fabricated in a 0.18-μm standard CMOS technology, and their DC, impulse and frequency responses were characterized. A 70 × 70 μm² PD with the new structure achieved a 3-dB bandwidth of 2.2 GHz in small signal at 5-V bias, whereas conventional lateral and vertical PIN PDs could only operate up to 0.94 GHz and 1.15 GHz, respectively. At 5-V bias, the impulse response of the new PD exhibited a full-width at half-maximum pulsewidth of 127 ps, versus 175 and 150 ps for the conventional lateral and vertical ones, respectively. At 15.5-V bias, the bandwidth of this new PD reached 3.13 GHz, with an impulse response pulsewidth of 102 ps. The responsivity of all prototype PDs was measured at approximately 0.14 A/W up to 10-V bias, which corresponded to a quantum efficiency of 20%. The responsivity of the new PD could be further increased to 0.4 A/W or 58% quantum efficiency, when operating in the avalanche region at 16.2-V bias.

I. INTRODUCTION

Demands for high-speed short-haul optical links are rapidly growing in recent years. For example, optical 10 Gigabit Ethernet [1] has become the major candidate for next generation local area networks. For storage networks and supercomputers, Fiber-Channel will be further developed to 10 Gbs [2]. Furthermore, inter- and intrachip optical interconnects are emerging as the ultimate solution to meet the bandwidth requirements in future high performance systems-on-chip (SoCs), such as multicore microprocessors [3], [4]. These systems require efficient detection of high-speed optical signals at 850 nm, the wavelength of choice in short-haul systems thanks to the low-cost vertical-cavity surface-emitting lasers (VCSELs) available at this wavelength. Discrete photodiodes (PDs) built in III–V compound semiconductors are typically employed to achieve the required large bandwidth [5]. Connecting the discrete PDs with the receiver electronics, however, introduces parasitic effects such as bondwire inductance and pad capacitance, which degrade the sensitivity and bandwidth of the overall system. As the number of PDs increases with the deployment of parallel optics or wavelength division multiplexing to further improve the aggregated system bandwidth, the interconnection bottleneck between the PD array and receiver electronics becomes increasingly problematic. Fully integrated optical receivers with PDs on the same chip will largely remove this limitation, and improve the overall system performance. Further, monolithic integration leads to lower cost and smaller size, and hence are very attractive for the target data communication applications.

Fully integrated optical receivers have been demonstrated in III–V technologies [5], [6]. With the ever-increasing system functionality and complexity, CMOS technologies, thanks to their integration and cost advantages, are becoming more attractive for optoelectronic integrated circuits (OEIC), which can now include amplifiers, decision circuits and demultiplexers [7]–[13]. The benefits of CMOS become even greater as more complex circuit functionalities, such as clock and data recovery and equalization, are integrated into these OEICs. For inter/intrachip optical interconnects, it is imperative that the integrated photonics devices including PDs are compatible with future CMOS technologies. Therefore, CMOS-compatible, high-speed, integrated silicon PDs are highly desirable and worth further investigation.

Unfortunately, the optical absorption coefficient of silicon is quite low at near-infrared wavelengths. Calculations using the standard photogeneration equations [14] show that the penetration depth of light in silicon is 16.5 μm at 850 nm. In typical CMOS technologies, the silicon substrate is much thicker (hundreds of μm) than that. Secondly, the doping concentration of silicon layers in CMOS technologies are typically quite high, and hence higher bias voltages are needed to deplete the active silicon layers. On the other hand, due to the high doping concentration, breakdown voltage of PN junctions in CMOS are fairly low, which limits the applicable reverse bias voltage on the integrated PDs. Hence, the entire penetration depth is not fully depleted in a typical integrated silicon PD. This causes the slow diffusion of minority carriers photogenerated deep inside the silicon substrate and reduces the PD bandwidth [15]. In addition, such low bias voltage applied results in weak electric field in the

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depletion region, and hence low drift velocity for the photogenerated carriers, far from reaching velocity saturation. Hence, the long carrier transit time further limits the achievable bandwidth of CMOS-integrated silicon PDs.

To overcome these limitations, one solution is to use a thinner silicon layer. This allows lower bias voltages to fully deplete the entire silicon layer, and remove the substrate diffusion problem. It also increases the drift velocity in the depletion region, and thus enhance the bandwidth of the device. On the other hand, this approach reduces the maximum achievable responsivity of PDs. Silicon-on-insulator (SOI) technologies provide such a thin silicon layer. With a 2.7-μm silicon layer on a sapphire substrate, Schow et al. demonstrated an SOI PD with a 3.4-GHz bandwidth and 24% quantum efficiency [16]. The relatively thick silicon layer, however, is unlikely to be compatible with SOI CMOS technologies, in which the top silicon layer is typically less than 200 nm to implement partially/fully depleted CMOS transistors [17]. Cسطاك et al. demonstrated silicon PDs built on an SOI substrate with a bandwidth of 15 GHz, thanks to a thinner silicon layer (200 nm) and a significantly sacrificed quantum efficiency (2%) [18]. As an evidence of the incompatibility with SOI CMOS, it is worth noting that the latest silicon OEICs resorted to discrete PDs flip-chip bonded to a standard SOI CMOS chip [13]. Similarly, thin layers of polysilicon, which are readily available in CMOS processes, can be used for high-speed PDs. In [19], a 6-GHz polysilicon PD was constructed between two heavily doped polysilicon layers. Again, due to the small thickness of the these layers, these PDs achieved only 0.2% quantum efficiency. Clearly, the material properties of silicon in CMOS technologies set the fundamental limit on the bandwidth-responsivity product of silicon PDs.

This leads to another solution, i.e., changing the photogeneration layer material. Germanium exhibits much stronger optical absorption than silicon at near-infrared wavelengths. Recently, Ge-on-Si PDs with 39-GHz bandwidth and 23% quantum efficiency [20], and Ge-on-SOI PDs with 29-GHz bandwidth and 34% quantum efficiency [21], both at 850 nm and low bias voltages, have been reported. Further assisted by a traveling-wave structure, a Ge-on-SOI waveguide PD achieved 31-GHz bandwidth and 71% quantum efficiency at 1550 nm [22]. CMOS compatibility of these devices, however, still remains challenging, and complex traveling-wave structures are likely needed to enhance the responsivity when thin Ge layers are used. SiGe PDs [23]–[25] can potentially be built in standard CMOS and BiCMOS technologies with the integration of silicon germanium (SiGe) layers, although the responsivity will likely be lower. Other more exotic PD structures, such as metal–semiconductor–metal [26], deep polysilicon trench [27], and resonant-cavity enhancement [28], were also demonstrated, but require significant process modifications and are incompatible with standard CMOS technologies.

Recently, silicon PDs integrated in standard CMOS technologies have been demonstrated with multi-GHz bandwidth and gigabit-per-second (Gbps) data rate at near-infrared wavelength. For example, vertical PIN PDs fabricated in a standard CMOS process achieved 1.7-GHz small-signal bandwidth with 49% quantum efficiency at 635 nm [29]. At 850 nm, 1-Gbps data rate was achieved by using a n-well guard ring to collect some of the diffusing carriers [30]. 500-Mb/s data rate was demonstrated, using a differential n-well diode, which had dark–light patterns to cancel some of the diffusion current [31].

Using shallow trench oxide and p-well in a standard CMOS process, 1.6-GHz bandwidth was achieved at 14-V bias with a responsivity of 0.74 A/W in the avalanche mode [32]. However, the speed of this PD structure is limited by the transit time of photogenerated carriers at lower bias voltages (At 5-V bias, this PD achieves 0.6-GHz bandwidth and 0.37-A/W responsivity with 54% quantum efficiency). In order to further improve the PD speed performance, the carrier transit time issue has to be addressed.

In this paper, we present a new PD structure in standard CMOS technology, using the available deep n-well layer, to enhance the electric field inside the substrate and hence reduce the carrier transit time in the depletion region. This technique enhances the bandwidth significantly. The paper is organized as following: In Section II, we discuss several topologies of CMOS integrated PDs, and present the new PD structure using deep n-well. In Section III, impulse response and small-signal measurement results of the prototype CMOS PDs are presented. Finally, in Section IV, we conclude the paper with a performance summary of the new PD structure, comparing with conventional structures.

II. PD DESIGN AND IMPLEMENTATION

A. New CMOS PD Structure Using Deep N-Well

Besides the material property and optical wavelength, performance (responsivity and bandwidth) of an integrated CMOS PD also strongly depend on its device structure, the choice of which is limited by the available silicon and dielectric layers as well as their thickness and doping profiles in a process technology. Therefore, it is worthwhile to distinguish two types of CMOS technologies. In a bulk-CMOS process, a moderately doped p-type substrate is typically used. The N+ region (drain/source for nMOS transistors), lightly doped n-well, and substrate form a vertical PIN PD [Fig. 1(a)]. Such a bulk-CMOS vertical PD generally exhibits a small bandwidth due to the slow diffusion of photogenerated carriers deep in the substrate.

In an epi-CMOS process, a lightly doped p-type epitaxial layer is grown on top of a heavily doped p-type substrate, mainly to prevent latch-up in CMOS circuits [33]. The epi-layer, which has higher resistivity than the heavily doped substrate, is used to pair with n-well to form the intrinsic region in a vertical PIN PD [Fig. 1(b)]. In such a PD structure, the electric field is largely confined inside the epi-layer, between the P+ substrate and N+ region on the surface. One advantage of epi-CMOS PDs is that when the epi-layer is thin enough, a low bias voltage can deplete the entire epi-layer, thanks to its low doping level. Further, the minority carrier recombination is faster in the P+ substrate than in the bulk CMOS case, and hence most photogenerated electrons inside the substrate recombine before diffusing into the depletion region [34], reducing the diffusion current effect. Therefore, epi-CMOS is more suitable for high-speed integrated PDs. In the following discussions, we assume that an epi-CMOS technology is used. However, if the epi-layer is too thin, the
substrate diffusion current becomes comparable to the photo-
generation current from the epi-layer, which then degrades the
PD bandwidth. Therefore, the thickness and doping level of the
epi-layer and substrate strongly affects the tradeoff between the
PD bandwidth and responsivity.

In addition to vertical PIN structures, a lateral PIN PD can
be constructed by alternating the p-type epi-layer and n-type
(n-well) regions in a lateral interdigitated fashion [7], [8], sim-
ilar to a multi-fingered MOSFET [Fig. 1(c)]. Now the finger
spacing affects the transit time of the photogenerated carriers.
The closer the fingers are, the faster electrons and holes drift to
the electrodes. On the other hand, the smaller the finger spacing,
the higher the parasitic capacitance, and hence the larger the
equivalent extrinsic $RC$ time constant. Assuming diffusion cur-
cent is not a concern, this structure is potentially faster than a
vertical PIN, given that the spacing between the fingers is prop-
erly selected. When the epi-layer is much thicker than the N+
regions though, the electric field close to the epi/substrate inter-
face is much weaker, and hence the drift velocity there is much
slower than close to the surface. This causes the PD bandwidth
to decrease to possibly even lower than a vertical PIN. Unfor-
tunately, the latter is typically the case for modern CMOS tech-
nologies.

In this study, we utilize deep n-well (DNW), an n-type
layer buried inside the epitaxial layer in epi-CMOS technolo-
gies. This layer is typically used to improve transistor isola-
tion and reduce substrate noise coupling in mixed-signal and
RF circuits [35]. A new PD structure can be implemented by
adding it inside the epi-layer in a lateral PIN structure, as shown
in Fig. 1(d). In such a structure, the DNW is connected to the
cathode through N+/n-well and creates two vertical PN junc-
tions: one with the now isolated p-type region on the surface
(called isolated p-region), and the other with the epi-layer and
substrate below. The upper one effectively becomes a hybrid lat-
eral–vertical PIN structure with a thinner depletion region than
without the DNW. The bottom PN junction can be used to iso-
late the upper one from the substrate and block the substrate
diffusion current [30]. If the substrate diffusion is not a major
concern, it can also be connected in parallel with the upper PN
junction. In this case, the electric field inside the lower depletion
region is much stronger than that without the DNW, and hence
leads to larger bandwidth even at lower bias voltages without
sacrificing responsivity. Overall, introducing DNW combines
the benefits of lateral and vertical PIN PDs, enhancing the band-
width and reducing the bias voltage needed for high-speed op-
eration. We call this new structure DNW PD in the rest of the
paper.

B. Test Chip Implementation

Several prototype PDs were designed and implemented on a
test chip in a standard 0.18-$\mu$m digital epi-CMOS technology.
These PDs had different structures with different active areas.
Vertical PIN PDs had 120 $\times$ 120 $\mu$m$^2$ active area, while lateral
and DNW PDs had 100 $\times$ 100 $\mu$m$^2$ and 70 $\times$ 70 $\mu$m$^2$ areas with
finger spacing of 1, 2, and 4-$\mu$m and finger width of 0.8-$\mu$m. In
the new DNW PDs, the DNW layer was connected to the fin-
gered N+ cathode through n-wells, and the P+ fingered anode
and p-type substrate were connected together to ground. A rel-
atively large active area was chosen for our devices to ensure

![Fig. 1. Cross-section of CMOS PD structures: (a) vertical PIN in bulk CMOS, (b) vertical PIN in epi-CMOS, (c) lateral PIN in epi-CMOS, and (d) new structure with deep n-well (DNW) in epi-CMOS. Only part of the PD is shown in (c) and (d) for clarity. All p-type substrates are connected to ground as in standard CMOS ICs.](image-url)
Fig. 2. Process parameters of the standard 0.18-μm epi-CMOS technology used for device fabrication, showing the cross section of one interdigitated section of the DNW PD structure. The doping concentration numbers are approximate average values.

Fig. 3. Effect of substrate doping concentration on the frequency response of the (a) vertical and (b) new DNW PD, at 850 nm illumination. All data are normalized according to the DC value.

good coupling with the incident light for more accurate DC responsivity measurement, although smaller device area would further improve the bandwidth. Each PD was connected to an output ground-signal-ground (GSG) pad, to apply the DC bias and measure the output signal. To facilitate the dark current measurement, each PD was implemented with a dummy duplicate with the active region covered with metal. The process parameters of the technology and the cross section of a prototype DNW PD are shown in Fig. 2.

C. Simulation Results

A 3-D device simulator, DA VINCI, was used to analyze photogeneration, electric field, charge distribution and small-signal frequency response of the prototype PDs. In the simulation, the output current was measured at the PD cathode, was connected to a 50-Ω load, and the anode was connected to ground. To reduce simulation time, the thickness of the silicon substrate was set to 40 μm, which was more than twice of the optical penetration depth (16.5 μm) at 850 nm, and hence would only introduce negligible error.

To evaluate the effect of the substrate, we varied the doping concentration of the P+ substrate of a vertical PIN PD. The results for different substrate doping levels at same bias voltage values (15 V) are shown in Fig. 3(a). The high frequency roll-off is determined by the carrier transit time and the parasitic capacitance, while the low-frequency drop is due to the substrate diffusion. When the substrate is lightly doped, the depletion region extends more into the substrate, improving responsivity. However, because the electric field becomes weaker into the substrate, the electrons collected deep in the substrate start drifting slowly and hence, reduce the high-frequency roll-off. Lower substrate doping concentration also increases diffusion length of the electrons, resulting in steeper drop at the low frequency. The same effect can be observed in the new DNW PD structure, as shown in Fig. 3(b). Also note that, the low-frequency
The roll-off point is higher than the vertical PD, thanks to the presence of DNW, which collects generated carriers from the substrate faster. In this epi-CMOS process, which has high substrate doping concentration ($5 \times 10^{18}$ cm$^{-3}$), PDs can potentially achieve larger bandwidth compared to a bulk CMOS technology, where substrate is lightly doped.

To demonstrate the advantages of the new structure, the electric field and potential distribution of lateral PIN and DNW PDs, each having 2-μm finger spacing (optimized for bandwidth) and 70 × 70 μm$^2$ area, are shown in Fig. 4. In both lateral and DNW PDs, the electric field is high enough to maintain velocity saturation for the generated electrons close to the silicon surface. Fig. 4(a) shows that the potential drops quite fast, and hence the electric field is very weak close to the epi-layer/substrate interface except at the step junction between the epi-layer and P+ substrate, as shown in Fig. 4(b). Because of the weak electric field, the generated carriers will drift slowly, degrading the bandwidth of the PD. In the DNW PD, the DNW layer introduces a high potential in the middle of epi-layer [Fig. 4(c)], and thus increases the electric field in the lower epi-layer [Fig. 4(d)]. This helps the electrons close to the epi/substrate junction be swept to cathode faster, close to velocity saturation. Compared to lateral PIN PD [Fig. 4(b)], DNW PD has larger depletion width and average electric field magnitude inside the active region [epi-layer, Fig. 4(d)].

Fig. 5 shows the small-signal frequency response for these 70 × 70 μm$^2$ lateral [Fig. 5(a)] and DNW PDs [Fig. 5(b)]. The results clearly show that using a DNW in the PD improves the bandwidth significantly (up to 4 GHz at 15 V). In particular, the bandwidth of the DNW PD is above 2 GHz even at a low bias voltage of 5 V, which is especially desirable for integrated optical receivers. As discussed in Section II.A, DNW combines the benefits of vertical PIN PD and lateral PIN PD, and achieves higher bandwidth with lower bias voltage values, without sacrificing responsivity. Table I presents all the simulation results for different bias conditions and PD structures at 850 nm. The responsivity for vertical PIN structure is slightly lower compared to lateral and new DNW PD ones because some carriers generated in the heavily doped N+ region on the surface recombine before reaching to the cathode.

III. TEST SETUP AND MEASUREMENT RESULTS

Three types of measurements were performed to characterize the PDs: DC (for responsivity and dark currents), impulse response, and small-signal frequency response. In these measurements, the test chip was glued to a custom-built printed circuit
board (PCB) using conducting epoxy, and hence the chip backside was connected to ground. The GSG pad of the PD under test was wire-bonded to a 50-Ω coplanar waveguide transmission line on the PCB, and connected to instruments through RF connectors at the edge of the PCB and coaxial RF cables. Note that no anti-reflection coating was applied on the prototype PDs.

A. Responsivity and Dark Current

In the DC measurement, a high speed VCSEL (Finisar HFE8004-103), with an optical power of 2 mW, was used as the light source at 850 nm. The emitted light was collimated and then focused onto the PD with two stages of lens. The spot size was adjusted to precisely cover the active region. A commercial silicon PIN diode (EOT ET-2030), with a bandwidth of 1.2 GHz and responsivity of 0.4 A/W at 850 nm, was used as a calibration reference for the optical power of the VCSEL. All results at 5-V bias are listed in Table II.

At 5-V bias, the responsivities were 0.132, 0.141, 0.146 A/W, for the 70×70 μm² PDs with DNW and finger spacings of 1, 2, and 4 μm, respectively corresponding to quantum efficiencies of 19–21%. Note that these results were 41% lower than the responsivity values from the simulation. Due to the lack of antireflection coating layer and the presence of a 8.5-μm thick oxide on top, 15% percent of the light was reflected, according to the calculations. In addition, due to the metal coverage ratio (29% for 2-μm finger spacing), the optical coupling loss was further increased to 37%, which is very close to the measurement results. It was evident that the larger the finger spacing, the less area covered by metals, and the higher responsivity. The 100×100 μm², 2-μm finger-spaced DNW PD yielded the same responsivity (0.142 A/W) and quantum efficiency of 20%, which showed that the incident light was well focused. The responsivity of the lateral PIN PDs was almost identical to the DNW PDs since the DNW does not change the depth of the photogeneration region. The 120×120 μm² vertical PIN PD achieved 0.135 A/W responsivity and 19.3% quantum efficiency.

The measured dark current values were 0.42, 0.46 and 0.40 nA for 1, 2, and 4-μm finger-spaced 70×70 μm² DNW PDs, respectively, at 5-V bias. The devices without DNW had slightly lower dark current than those with DNW, due to smaller junction area. On the other hand, larger PDs exhibited larger dark current values due to increased junction area. In particular, the results for the 2-μm finger-spaced DNW PD are shown in Fig. 6. Its dark current was below 1 nA until 13-V bias, and the

![Fig. 5. Normalized frequency response of (a) 2-μm finger-spaced lateral PIN PD, (b) 2-μm finger-spaced DNW PD in DA VINCI at 850 nm.](image)

![Fig. 6. Measured responsivity and dark current for the 70×70 μm², 2-μm finger-spaced new DNW PD when sweeping the bias voltage.](image)

<table>
<thead>
<tr>
<th>Type</th>
<th>Area (μm²)</th>
<th>Finger (μm)</th>
<th>Bias (V)</th>
<th>R_{dc} (A/W)</th>
<th>I_{dark} (nA)</th>
<th>BW (GHz)</th>
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<tr>
<td>DNW</td>
<td>70×70</td>
<td>2</td>
<td>5</td>
<td>0.24</td>
<td>0.48</td>
<td>2.2</td>
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<td></td>
<td></td>
<td>10</td>
<td></td>
<td>0.24</td>
<td>0.65</td>
<td>3.2</td>
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<tr>
<td></td>
<td></td>
<td>15</td>
<td></td>
<td>0.25</td>
<td>0.72</td>
<td>4.0</td>
</tr>
<tr>
<td>Lat.</td>
<td>70×70</td>
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<td>5</td>
<td>0.23</td>
<td>0.32</td>
<td>0.75</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>0.23</td>
<td>0.44</td>
<td>1.85</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td></td>
<td>0.24</td>
<td>0.63</td>
<td>2.95</td>
</tr>
<tr>
<td>Vert.</td>
<td>120×120</td>
<td>-</td>
<td>5</td>
<td>0.21</td>
<td>0.42</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>0.21</td>
<td>0.78</td>
<td>1.95</td>
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<tr>
<td></td>
<td></td>
<td>15</td>
<td></td>
<td>0.21</td>
<td>0.79</td>
<td>2.1</td>
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</table>

Table I: Summary of simulation results for prototype PDs at 850 nm.
Table II
SUMMARY OF MEASUREMENT RESULTS AT 850 nm

<table>
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<tr>
<th>Type</th>
<th>Area (μm²)</th>
<th>Finger (μm)</th>
<th>R_{dc} (A/W)</th>
<th>I_{dark} (nA)</th>
<th>τ_{FWHM} (ps)</th>
<th>T_f (ps)</th>
<th>IBW (GHz)</th>
<th>BW (GHz)</th>
<th>QE×BW (GHz)</th>
<th>C (pF)</th>
<th>RC-BW (GHz)</th>
<th>BW (GHz)</th>
<th>Gain (dB)</th>
<th>Gain×BW (GHz)</th>
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<tr>
<td>DNW</td>
<td>70x70</td>
<td>1</td>
<td>0.132</td>
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<td>162</td>
<td>168</td>
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<td>1.64</td>
<td>0.317</td>
<td>0.96</td>
<td>3.32</td>
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<td>2.97</td>
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<td>Lateral</td>
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<td>0.43</td>
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<td>276</td>
<td>0.72</td>
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<td>0.188</td>
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<tr>
<td>DNW</td>
<td>70x70</td>
<td>2</td>
<td>0.141</td>
<td>0.46</td>
<td>127</td>
<td>147</td>
<td>2.08</td>
<td>2.19</td>
<td>0.452</td>
<td>0.80</td>
<td>3.70</td>
<td>3.15</td>
<td>2.84</td>
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<tr>
<td>DNW</td>
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<td>0.145</td>
<td>0.41</td>
<td>210</td>
<td>382</td>
<td>0.67</td>
<td>1.01</td>
<td>0.210</td>
<td>1.53</td>
<td>2.00</td>
<td>1.55</td>
<td>0.2</td>
<td>1.65</td>
</tr>
<tr>
<td>Vert.</td>
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<td>-</td>
<td>0.135</td>
<td>0.48</td>
<td>150</td>
<td>155</td>
<td>1.52</td>
<td>1.15</td>
<td>0.227</td>
<td>0.77</td>
<td>3.88</td>
<td>1.61</td>
<td>0.2</td>
<td>1.65</td>
</tr>
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</table>

τ_{FWHM}: full width half maximum impulse width , T_f: 10%-to-90% fall time , QE: Quantum efficiency , Gain: Avalanche responsivity gain
BW: small-signal bandwidth , RC-BW: external PD parasitics limited BW

Fig. 7. (a) Impulse responses and (b) their DFT spectra of the 70×70 μm², 2-μm finger-spaced lateral and DNW PDs. The measurements are done under 850-nm illumination and at 5-V bias.

breakdown voltage was 16.4 V. The responsivity increased to 0.4 A/W (58% quantum efficiency) at 16.2 V. Further increase in the bias voltage up to 16.3 V helped the PD to have 0.7-A/W responsivity with a quantum efficiency of 100% when operating in the avalanche mode, but the dark current also increased to 3 μA.

B. Impulse Response

In the impulse response measurements, a tunable mode-locked Ti:Al₂O₃ femtosecond pulsed laser, operating between 700 and 1000 nm, was used as the light source with a repetition rate of 76 MHz. The pulsewidth was 100-fs, and could be treated as an impulse function in the PD measurements. The output of the PDs was fed into a digital sampling oscilloscope with a 3-dB bandwidth of 20 GHz. The average incident power on the PD was 0.27 mW at 850 nm, which corresponds to a peak power of 33.75 W and optical pulse energy of 3.55 pJ. The impulse response results were then converted to frequency response using discrete Fourier transform (DFT).
Fig. 10. (a) Bandwidth bias voltage dependence (b) normalized avalanche gain and bias voltage dependence of different PD structures. The responsivity values are normalized to 0-V bias condition. Lateral and DNW PDs are 2-μm finger spaced and have 70 × 70 μm² area. Vertical PIN PD has 120 × 120 μm² area.

Fig. 9. Small-signal frequency response of the new DNW PD for different bias voltages. Values are normalized to 0-V bias condition. 0 dB corresponds to the responsivity value of 0.14 A/W.

C. Small-Signal Frequency Response

In the small-signal measurement, the light source was the aforementioned 10-Gb/s 850-nm VCSEL, driven by one port of a vector network analyzer (VNA), and the output was received by the second port of the VNA. In the VNA calibration, the reference plane was set at the RF connectors of the VCSEL and PD PCBs, to exclude cable loss and bias tees. It was assumed that the PCB traces and bond-wires would have negligible effect on the frequency response within the PD’s 3-dB bandwidth. All the measurement results are summarized in Table II.

In Fig. 9, the small-signal frequency response of 70 × 70 μm² 2-μm finger-spaced DNW PD is plotted. The PD bandwidth was 2.2 GHz at 5-V bias and increased up to 3.13 GHz at 15.5 V. In the avalanche mode, the PD’s responsivity increased by 3 dB at 15.5 V, and more than 6 dB at 16 V. However, the bandwidth started decreasing after 15.5-V bias voltage. At 16 V, the bandwidth dropped to 2.8 GHz, and at 16.2 V, it decreased to 2.23 GHz with a responsivity gain of 8 dB. Fig. 10 compares the DNW PD with the conventional structures in terms of bandwidth [Fig. 10(a)] and avalanche responsivity gain [Fig. 10(b)] with respect to bias voltage. The DNW PD had larger bandwidth, whereas lateral PIN and DNW PDs achieved larger avalanche gain than vertical PIN PD.

To analyze the extrinsic RC effect, we also measured the parasitic capacitances of the PDs. This impedance measurement was performed by one-port S-parameter measurements using the VNA, with no light shined on the PDs. The bond-wire inductance, pad capacitance and PCB trace loss, which do not affect the performance of fully-integrated silicon PDs, were de-embedded in the measurement by VNA calibration. We observed that the capacitance of DNW PD had slightly lower capacitance than the lateral one without DNW. The extrinsic RC time constant was calculated by multiplying series resistance of the PD and 50 Ω the port impedance with the parasitic capacitance of the PD, and the RC limited bandwidth (RC-BW) is shown in Table II. 2-μm finger-spaced DNW, lateral, and vertical PIN PDs had RC limited bandwidth of 3.7, 3.5, and 3.7 GHz, respectively, at 5-V bias. These results show that the measured small-signal responses were mainly determined by drift and substrate
diffusion effects, but still affected by extrinsic $RC$ time constant. By reducing the device size, the DNW PD can potentially achieve even larger bandwidth.

Table II summarizes all the DC, impulse, and frequency response measurement results at 850 nm illumination and 5-V bias. It is evident that the 2-$\mu$m finger-spaced DNW PDs achieved the largest bandwidth among the others. Further, both 1-$\mu$m and 2-$\mu$m finger-spaced DNW PDs achieved larger bandwidth (above 2.5 GHz) than the 4-$\mu$m finger-spaced one, which is mainly limited by drift time. In addition, the quantum efficiency-bandwidth product at 5-V bias and avalanche gain-bandwidth product at 15.5-V show that 2-$\mu$m finger-spaced DNW PD achieved the highest performance overall.

IV. CONCLUSION

The proposed new PD structure with deep n-well combines the advantages of vertical and lateral PIN devices, enhances the electric field inside the epi-layer, and thus increases the drift speed of electrons at the epi-layer/substrate interface. Therefore, it can improve the PD bandwidth without sacrificing the responsivity, and enables high speed photodetection at low bias voltages. Several prototype PDs, including conventional vertical, lateral and the proposed DNW PDs, were implemented in a standard epi-CMOS technology, and characterized by DC, impulse response and small-signal frequency response measurements. A DNW PD with an area of $70 \times 70$ $\mu$m$^2$ achieved a small-signal 3-dB bandwidth of more than 3 GHz at 15-V bias, significantly higher than the conventional lateral and vertical PIN structures (1.85 and 1.61 GHz). At 5-V bias, the same DNW PD achieved 2.2-GHz bandwidth, versus about 1 GHz for the lateral and vertical PIN PDs. The DNW PD’s bandwidth showed little wavelength dependence between 750 and 850 nm. At 850 nm, its responsivity was measured at 0.14 A/W, corresponding to a quantum efficiency of 20% when biased below 10 V, and increased to 0.4 A/W or a quantum efficiency of 58% at 16.2-V bias. Its dark current maintained at the 0.5-nA level at 5-V bias, similar to the vertical and lateral PIN PDs. These results demonstrated a new approach to build higher-speed integrated silicon PDs with good responsivity, in a standard CMOS technology without major process modifications.

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REFERENCES

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